

CLAIMS

What is claimed is:

1. A semiconductor device comprising:

- a semiconductor substrate having a first surface;
- a pair of active areas formed in the first surface;
- a deposited oxide layer proximate the active areas; and
- a gate over the first surface between the pair of active areas.

2. The semiconductor device of Claim 1, further comprising a thermal oxide layer disposed between the deposited oxide layer and the first surface of the semiconductor substrate.

3. The semiconductor device of Claim 1, wherein the thickness of the deposited oxide layer varies across the active areas.

4. The semiconductor device of Claim 1, wherein the active areas are n-doped regions.

5. The semiconductor device of Claim 1, wherein the semiconductor substrate is P-type silicon.

6. The semiconductor device of Claim 1, wherein the gate is comprised of a gate oxide layer and a poly silicon layer.

7. A method of making a semiconductor device comprising:

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depositing a layer of oxide proximate a first surface of a semiconductor substrate;

forming a gate oxide layer on the first surface, adjacent to the deposited oxide layer;

forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer;

forming a gate electrode by depositing a conductive layer over the gate oxide layer;

depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer; and

forming electrical contacts to the pair of active areas and the gate electrode.

8. The method of Claim 7, further comprising thermally growing a thermal oxide layer before depositing the layer of oxide on the first surface of the semiconductor substrate.

9. The method of Claim 7, wherein the semiconductor substrate is P type silicon.

10. The method of Claim 7, wherein the active areas are formed by impurity implant and diffusion.

11. The method of Claim 7, wherein the active areas are n-doped regions.

12. The method of Claim 7, wherein the conductive layer over the gate oxide layer is polysilicon.

13. The method of Claim 7, wherein the dielectric layer is silicon dioxide.

14. An print cartridge comprising:

a reservoir of fluid; and

a print head, said print head including:

a semiconductor substrate having a first surface;

a pair of active areas formed in the first surface;

a deposited oxide layer proximate the active areas; and

a gate electrode over the first surface between the pair of active areas.

15. The print cartridge of Claim 14, further comprising a plurality of thin layers disposed over the first surface, the thin film layers including fluid ejection elements.

16. The print cartridge of Claim 15, further comprising:

an orifice layer disposed over the thin film layers, the orifice layer defining a plurality of fluid ejection chambers.

17. The print cartridge of Claim 15, wherein said fluid ejection elements are heater resistors.

18. The print cartridge of Claim 16, wherein said fluid ejection elements are piezoelectric actuators.

19. A method of manufacturing a fluid ejection device, the method comprising:

forming first and second active areas in a first surface of a semiconductor substrate;

depositing a current prevention layer on the first surface in between the first and second active areas;

forming a gate oxide on the first surface adjacent to the second active area; and

forming a gate electrode for a drive transistor of the fluid ejection device on the gate oxide, wherein the current prevention layer minimizes current flow between the first and second active areas and the gate electrode.

20. The method of Claim 19, wherein the current prevention layer is a dielectric.

21. The method of Claim 19, wherein the current prevention layer is an oxide.